REMARKS

Claim 1 - 7 remain pending in the present application. The rejections set forth in the Office Action is respectfully traversed below.

Rejections under 35 U.S.C. §102

Independent claim 1 was rejected under 35 U.S.C. §102 over different prior art references. It is submitted that nothing in the prior art teaches or suggests all the features recited in the present claimed invention, as amended.

Yamasaki

Claim 1 was rejected under 35 U.S.C. §102 over **Yamasaki et al.** (USP 5,973,554). However, **Yamasaki** does not disclose a common power supply line to which the power supply lines are connected, as recited in amended claim 1.

Lu

Claim 1 was rejected under 35 U.S.C. §102 over **Lu et al.** (USP 6,100,573). However, **Lu** also does not disclose a common power supply line to which the plurality of power supply lines are connected.

Correale

Claim 1 was rejected under 35 U.S.C. §102 over **Correale, Jr.** (USP 5,789,807). However, stitch line 503 (see Fig. 5A) appears to disclose a ***serial*** connection between power supply lines between layer M3 and M1. The present claimed invention requires the power supply lines at different layers of a multilayer wiring structure to be connected in ***parallel***. Fig. 6 of **Correale** and the corresponding description in col. 4, lines 35-30 indicate that there is only a ***serial*** connection between the power supply line at one layer M3 to another layer M1. Indeed, **Correale** requires this ***serial*** connection in order to increase the metal decoupling capacitance significantly over the vertical sandwich arrangement depicted in Fig. 3. Therefore, the rejection based on **Correale** should be withdrawn.

Mimoto

Claims 1-7 were rejected under 35 U.S.C. §102 over **Mimoto et al.** (USP 6,326,693). Only the embodiments depicted in Figs. 14 and 15 appear to disclose the use of a common power supply line, *e.g.*, 5b. However, the plurality of power supply lines, *e.g.* 41 and 42 which are connected to the common power supply line 5b are disposed at the ***same*** level in the multilayer wiring structure. Power supply lines 33 and 34 are also *electrically* connected to the common power supply line 5b (but actually physically connected to common power supply line 5a at a *different level* in the multilayer wiring structure). Nevertheless, power supply lines 33 and 34 are both located at the same level and are not electrically connected in *parallel* to power supply lines 41 and 42. In other words, the embodiments described by way of Figs. 14 and 15 do not disclose the claimed plurality of power

supply lines "disposed at different layers of the multilayer wiring structure" **and** "being connected in **parallel** to each other." For at least these reasons, **Mimoto** does not teach or suggest the present claimed invention.

Rejections Under 35 U.S.C. §103

Claims 2-7 were rejected under 35 U.S.C. 103 over **Correale**. The Office Action alleged that the stitches appear to have a width larger than that of the power supply lines in layers M1 and M3 (see Fig. 5A). However, as mentioned above, the power supply circuits described in **Correale**, having lines in different layers, only appear to be connected ***serially***- not in ***parallel***. Therefore, notwithstanding whether or not the stitches (*e.g.* 503) can constitute the present claimed common power supply line, **Correale** does not teach or suggest all the features recited base independent claim 1. Therefore, the rejections of claims 2-7 wish depend directly or indirectly from independent claim 1, should be withdrawn.

Summary

Nothing in the cited prior art, either alone or in combination, teaches or suggests all the features recited in the present claimed invention, as amended. If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosures: Version with markings to show changes made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE 10/090,610

IN THE CLAIMS:

Claim 1 has been **AMENDED** to read as follows:

1. (AMENDED) A multilayer wiring structure for semiconductor devices, comprising:

a semiconductor substrate;

at least one active region supplied with an electric power from a power-supply potential;

[and]

a plurality of power-supply lines for supplying with the electric power to said active region therethrough, said power-supply lines disposed at different layers of the multilayer wiring structure on said semiconductor substrate and being connected in parallel to each other; and

a common power-supply line provided between said power-supply potential and said active region, the common power-supply line being connected to the power-supply lines and having a current-carrying capacity larger than that of each of the power-supply lines.